ABSTRACT OF THE DISCLOSURE

A chip structure comprising a semiconductor substrate, a plurality of dielectric layers, a plurality of circuit layers, a passivation layer, a metal layer and at least a bump. The semiconductor substrate has a plurality of electronic devices positioned on a surface layer of the semiconductor substrate. The dielectric layers are sequentially stacked on the semiconductor substrate and have a plurality of via holes. The circuit layers are disposed on one of the dielectric layers, wherein the circuit layers are electrically connected with each other through the via holes and are electrically connected to the electronic devices. The passivation layer is disposed over the circuit layers and the dielectric layers, wherein the passivation layer comprises an opening that exposes one of the metal layers. The metal layer is disposed over the passivation layer, wherein the metal layer comprises at least a bump pad and at least a testing pad, the bump pad electrically connecting with the testing pad. The bump is disposed on the bump pad.